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Modeling Study on the Solder Joint Reliability of a Leadframe Package under Powered Thermal Cycling

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Author's contribution

The sole author designed, analysed, interpreted and prepared the manuscript.

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ABSTRACT

This paper aims to present a thermo-mechanical modeling approach to predict the solder joint reliability of a leadframe-based package under powered thermal cycling (PTC) test from -40°C to 105°C. The study involves modeling the PTC condition as a standard thermal cycling with a modified temperature boundary to account for the temperature increase due to the applied power to the device package mounted on board. The temperature ramp and dwell times were maintained. Based on the finite element analysis (FEA) results and comparison with actual data, modeling a PTC as a modified thermal cycling process provides a good prediction of the solder joint life. The analysis is simpler and would be beneficial for getting quick assessments of new leadframe package designs.

Keywords: Solder joint reliability; thermomechanical modeling; powered thermal cycling; finite element analysis; leadframe package.

1. INTRODUCTION

Solder joint reliability of lead frame packages is usually evaluated under thermal cycling. This is to assess the reliability of solder joints when subjected to alternating cold and hot temperature conditions in actual use. In automotive and high power applications, heat generated in the integrated circuit (IC) die increases significantly. For such applications, leadframe-based

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packages are commonly used because of its superior thermal performance compared to laminate substrate-based packages. The exposed pad of the leadframe acts as a heatsink for removing heat from the die. The package is mounted on the printed circuit board (PCB) using solder joint material to establish electrical connection between the IC package leads and the PCB pads and conductive traces. The soldered connection of the leadframe under the die also serves as a thermal path for heat dissipation. Fig. 1 shows such package being soldered to the PCB.

The solder joint is subjected to higher levels of stress during temperature cycling on board (TCoB) because of the differences in the coefficient of thermal expansion (CTE) of the materials. Solder crack is the usual manifestation of the problem and this crack propagates until the solder joint connection fails completely causing electrical and mechanical connection problem between the package and the PCB.

Many of the solder joint fatigue studies [1-6] are involving thermal cycling only in which there is no power supplied to the package when it is subjected to thermal cycles in a thermal chamber. However, in actual device application, power is supplied to the device while it experiences alternating hot and cold temperatures. Some semiconductor manufacturers require the solder joint to survive powered thermal cycling for a certain number of cycles. In this study, solder joint reliability modeling was performed as a standard thermal cycling with a modified temperature boundary to account for the temperature increase due to power cycling.

2. SOLDER JOINT RELIABILITY MODELING

Solder joint reliability modeling is commonly done using finite element analysis (FEA). This computer simulation enables faster evaluation of design options before the actual semiconductor package is built. It is also very useful in narrowing down available package design choices so that only those with expected better solder joint reliability would be built. The prediction of solder life is based on life prediction equation developed from actual experiments as well as the solder constitutive model for a certain solder material used.

2.1 Solder Constitutive and Fatigue Life Prediction Models

Constitutive models describe the material responses to various loading conditions and provide the stress–strain relationship of the material. For solder, there are different constitutive models commonly used in the microelectronics industry. One previous study [7] implemented four different models including elastic-plastic (EP), elastic-creep (Creep), elastic-plastic-creep (EPC) and viscoplastic Anand’s (Anand) models in modeling and simulation to investigate solder constitutive model effect on solder fatigue life and stress-strain response. Based on fatigue life prediction, it was shown that Creep, EPC and Anand models are suitable for thermal cycling simulations.

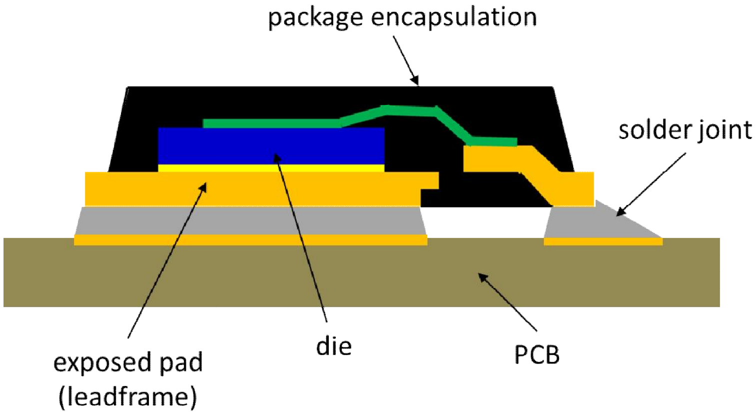

Fig. 1. Leadframe package mounted on a PCB

However, for SAC solders (e.g. SAC 305, SAC405, and SAC387), the hyperbolic sine creep equation is commonly used to model the solder's temperature and time-dependent creep behavior. It is defined as [7,8]:

$$\dot{\varepsilon}_c = C_1 \frac{G}{T}\left[\sinh\left(\alpha \frac{\sigma}{G}\right)\right]^n \exp\left[\frac{-Q}{kT}\right] \qquad (1)$$

When using ANSYS FEA software in doing the analysis, the creep strain rate is simplified and rewritten as:

$$\dot{\varepsilon}_c = C_1[\sinh(C_2\sigma)]^{C_3} \exp\left[\frac{-C_4}{T}\right] \qquad (2)$$

The C_1, C_2, C_3 and C_4 are material constants, which are the required inputs in the ANSYS FEA analysis software to define the creep strain rate of the solder material considered. Table 1 gives the input for ANSYS hyperbolic sine creep model used in this study.

Table 1. Constants for Sn-3.8Ag-0.7Cu Solder [8]

C_1	C_2	C_3	C_4
3.2e4	0.037	5.1	6524.7

The fatigue life prediction could either be based on strain or strain energy. However, Che et al [9] showed that the energy-based fatigue model resulted in accurate and reasonable fatigue life prediction compared to strain-based fatigue model. And in order to reduce the stress concentration effect, the volume-averaging method is typically used in parameter extraction from simulation results for solder fatigue life prediction [10]:

$$W_{cr} = \frac{\sum(W_{cri}\, V_i)}{\sum V_i} \qquad (3)$$

The volume-averaged accumulated strain energy density per cycle (W_{cr}) in equation (3) is implemented on the results in ANSYS software. Once the accumulated strain energy density per cycle is obtained from the model, the characteristic life in terms of the number of thermal cycles, Nf (63.2% accumulative failure), can be calculated by the following correlation for SnAgCu(SAC) solders [11]:

$$N_f = 345 W_{cr}^{(-1.02)} \qquad (4)$$

The fatigue correlation above, which is also known as Schubert's correlation model, has been found to have good prediction accuracy for BGA (ball grid array) laminate-based packages but not for leadframe-based packages like QFN (quad flat no lead). Another study [12] showed that a different fatigue correlation model would work well with solder fatigue life prediction for QFNs:

$$N_f = 741.37 W_{cr}^{(-0.3902)} \qquad (5)$$

2.2 Finite Element Analysis of the Solder Joint Reliability

In the standard thermal cycling finite element analysis (FEA), the temperatures applied are the same as the temperature of the thermal chamber since there is no power supplied to the device. Fig. 2 shows the temperature profile (-65°C to 150°C) for the standard thermal cycling analysis done during the leadframe package development. In this specific study, the dwell time was 20 minutes and the ramp time was 10 minutes or 1 thermal cycle per hour for the baseline condition. Three thermal cycles were simulated since this is the number of cycles in which the accumulated strain energy density or plastic work accumulation is already stable and the change becomes minimal [13].

On the other hand, the powered thermal cycling (PTC) was simulated as a standard thermal cycling with an increase of 30°C above the chamber temperature as indicated in Fig. 3. The thermal chamber temperature was at -40°C and 105°C. During each thermal chamber temperature cycle, there were seven power component cycles resulting in the 30°C temperature rise to the solder joint. In the analysis for this powered thermal cycling, the temperatures applied were -40°C and 135°C considering the extreme temperature boundaries when power is supplied to the device during thermal cycling.

The thermal cycling conditions used in the solder joint reliability analysis of the board-mounted power leadframe package are summarized in Table 2. The first one (Standard TC1) is the standard thermal cycling condition described earlier. An additional standard thermal cycling condition (Standard TC2) was included. This is also called thermal shock since the ramp time is very short but still no power is supplied to the device during thermal cycling. The third TC condition (Powered TC) is the one where power is supplied to the device during thermal cycling.

The different TC conditions were applied to a non-linear, half symmetry finite element model shown in Fig.4. The package modeled is having 4 leads and a die pad. The solder joint under the leadframe die pad is simplified with no solder fillet included. However, the solder joint connecting the package leads to the PCB has the solder fillet included since it is a critical joint and the model must be close as possible to the actual solder joint shape for accuracy of results.

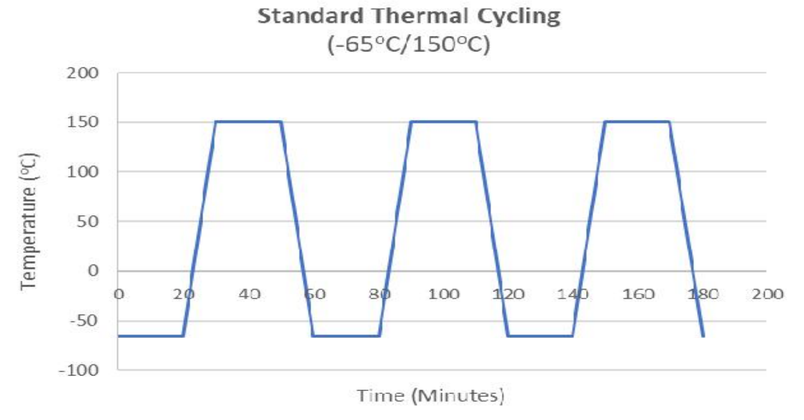

Fig. 2. Standard thermal cycling (TC) profile

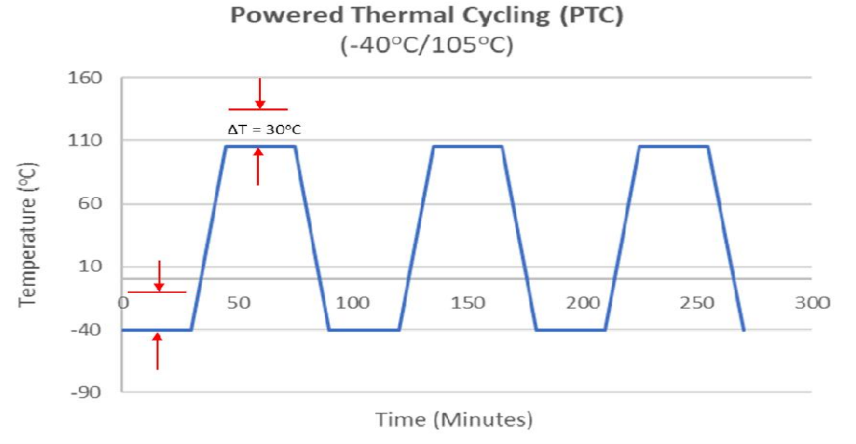

Fig. 3. Powered thermal cycling (PTC) profile

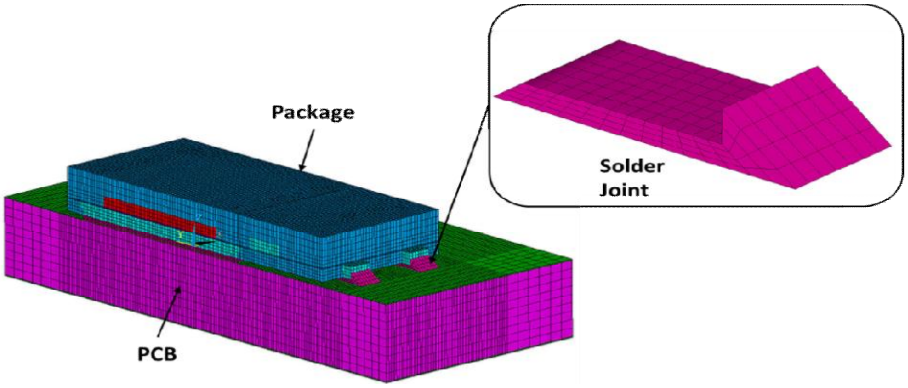

Fig. 4. Finite element model of the leadframe package mounted on PCB

Table 2. Thermal cycling conditions

TC condition	Chamber temperature (°C)	Temperature applied in the analysis (°C)	Dwell/ ramp (Minutes)
Standard TC1	-65° C/150° C	-65° C/150° C	20/10
Standard TC2	-40° C/125° C	-40° C/125° C	30/0.17
Powered TC	-40° C/105° C	-40° C/135° C	30/15

3. RESULTS AND DISCUSSION

The solder joint reliability modeling result is shown in Fig. 5 for the critical solder joint. It shows the creep strain energy density contour plot of that solder joint connection to the PCB after subjecting the board-mounted package to 3 thermal cycles. This corner joint was selected for the solder life cycle calculation in this study. The critical solder joint is located at the package corner and is the one expected to fail earlier than the other joints. The volume-averaging technique presented earlier was implemented to get the accumulated creep strain energy density per cycle for the top solder material interface layer.

From the accumulated strain energy density per cycle obtained, the characteristic life was calculated using the fatigue life prediction equation established for QFN solder joint [12]. Since the solder joint reliability requirement (2,000 cycles) was the number of cycles to first failure and not the characteristic life of the solder joint, the characteristic life was instead normalized against the baseline model result that showed no failure at 2,000 cycles. Fig. 6 shows the normalized solder fatigue life comparison. The baseline is the standard TC condition (-65°C/150°C) used during the development of the leadframe package considered in this study. It has a normalized solder life of 1.0 as a baseline. As shown in the normalized results, the powered TC condition applied gives the highest solder life and this means that this condition induces the lowest stress to the solder joint. The standard TC condition (TC1) is the one giving the lowest solder life and can be considered to be the worst TC condition giving the highest stress to the solder joint among the 3 thermal cycling conditions used.

Comparing the solder joint reliability modeling results with the actual data shown in Table 3, it can be observed that the solder life trend is the same. The modeling results are in good agreement with the actual data. The powered TC is also showing the highest solder life. This implies that the powered TC can be modeled as a standard TC and still provides valid results.

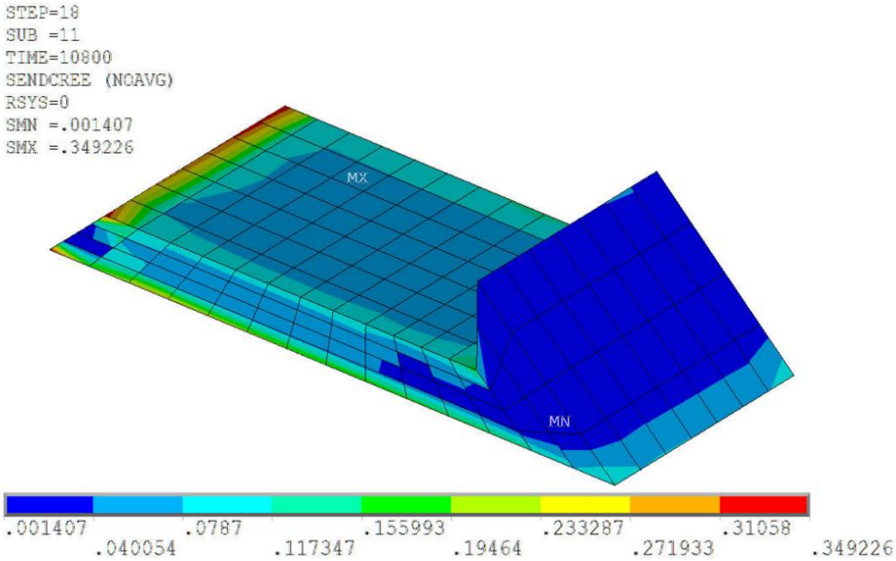

Fig. 5. Creep strain energy result of the solder joint after 3 thermal cycles

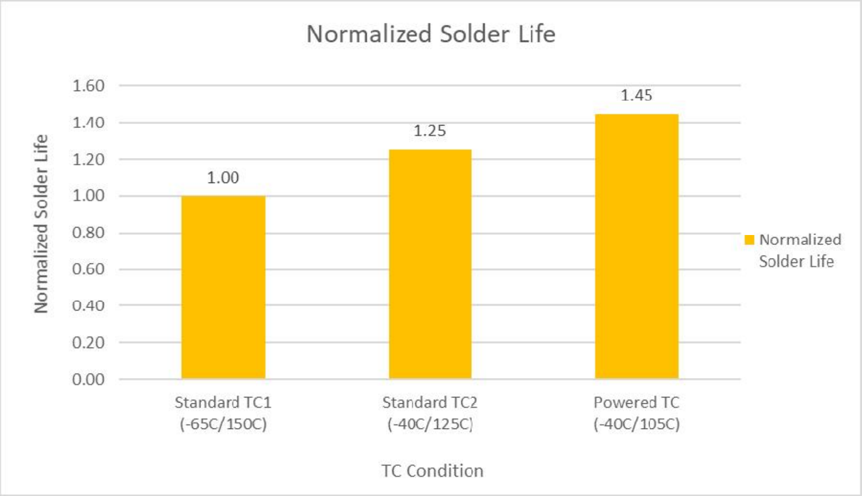

Fig. 6. Normalized solder fatigue life comparison

Table 3. Solder joint reliability results based on actual data

TC condition	Actual result
Standard TC1 (baseline)	PASSED (≥2,000 cycles)
Standard TC2	PASSED (~2,500 cycles *)
Powered TC	PASSED (~3,500 cycles *)

** Data (number of cycles) at ~50% actual crack length*

4. CONCLUSION

Solder joint reliability modeling of the leadframe package under powered thermal cycling (PTC) could be done as a standard thermal cycling process with a modified temperature boundary applied during the analysis in consideration of the temperature rise caused by power cycling during each chamber temperature cycle. This modeling approach provides a good prediction of the solder joint life of leadframe package mounted on board. The modeling is simpler and would be useful for getting quick assessments and narrowing down selections of several leadframe package design options.

DISCLAIMER

The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

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COMPETING INTERESTS

Author has declared that no competing interests exist.

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