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Enhanced Wirebonding Technique on QFN Device with Critical Die Reference

Jonathan C. Pulido[1*] and Frederick Ray I. Gomez[1]

[1]New Product Development & Introduction, STMicroelectronics, Inc., Calamba City, Laguna 4027, Philippines.

Authors' contributions

This work was carried out in collaboration between both authors. Both authors read, reviewed and approved the final manuscript.

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ABSTRACT

Wirebonding is one of the most challenging assembly manufacturing processes in semiconductor packaging industry. This paper discussed the wirebonding challenge and the solution to mitigate misplaced ball issues and prevent pattern recognition alignment errors. Parameter optimization particularly on wirebond looping was done to ensure that the silicon die's L-fiducial is visible and not obstructed by the wires, which is the operator point or die reference of the unit during wirebonding setup. Ultimately, the optimized wirebonding parameter prevented the pattern recognition alignment error and misplaced ball issues during the lot process. For future works, the configuration and technique could be applied on packages with the similar situation.

Keywords: Die reference; J-wire; looping profile; pattern recognition; wirebonding process.

1. INTRODUCTION

Quad-flat no-leads multi-row (QFN-mr) leadframe package is commonly used in semiconductor packaging industry due to its high-density input/output (I/O) capability. QFN-mr device can be found on various applications such as in hard disk drives and car infotainment. With continuous technology trends and breakthroughs including the QFN platform, challenges in assembly

**Corresponding author: Email: jonathan.pulido@st.com;*

manufacturing are expected [1-4]. On top of the technology innovation, it has been a common challenge in semiconductor packaging the criticality of wirebonding process [5-9]. Wirebonding is defined as the process of creating electrical interconnection between the semiconductor die and the I/O leads using bonding wires.

For the device in focus, two different programs in one die for wirebonding are required with the first wire group having 1 mil wire size and the second wire group of 2 mil size. During wirebonding process, an L-fiducial of the semiconductor die as shown in Fig. 1 is used as the reference for pattern recognition alignment.

It is important that the wirebonding reference is not obstructed especially during the second wirebonding sequence. Fig. 2 shows the actual image in the machine with the L-fiducial reference not anymore visible after the first wirebonding sequence.

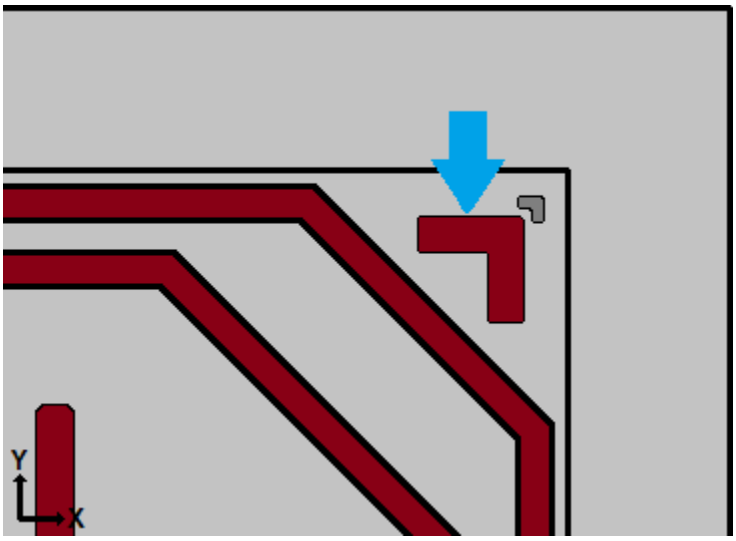

Fig. 1. Part of silicon die with the L-fiducial for wirebonding reference

Fig. 2. L-fiducial obstructed after completion of first wirebonding sequence

As emphasized, it is critical during the second wirebonding sequence that the L-fiducial reference is visible for the machine's pattern recognition system in order to prevent misplaced bond ball issues caused by the alignment error. This paper presents the technique to ensure flawless wirebonding operation with two programs for the QFN-mr device.

2. METHODS AND RESULTS

An overview of the assembly process flow applicable for the device in focus is shared in Fig 3, with the highlighted process concerned. There are two wirebonding sequence programs as there are two wire sizes for the device. The silicon die's L-fiducial is used as the reference for both wirebonding sequences.

As earlier shown in Fig. 2, the L-fiducial is not visible after the first wirebonding sequence, thus the setup for the second wirebonding sequence could not be completed. The die reference was initially suggested to temporarily assign to other area, but the machine program did not recommend it. Hence, wirebond parameter optimization was comprehensively done. The loop parameter was adjusted from the standard loop to the J-wire loop as depicted in Fig. 4.

With the enhanced wirebonding technique of applying J-wire loop on the specific wire, the L-fiducial was kept unobstructed. Fig. 5 shows the actual image in the machine, with the L-fiducial reference being visible and not obstructed after the first wirebonding sequence.

Note that adjusting the loop parameter is critical, such that after adjusting the parameter, visual inspection was done on the unit. This was done to check the actual wirebonding result for possible wire-to-wire issue and found none. Loop height measurement also passed the requirement.

With the J-wire loop implementation on the specific wire, no more pattern recognition alignment error occurred as shown in Fig. 6 with the L-fiducial kept visible at all times. Also, no occurrence of the misplaced ball on pad was observed during lot process, and was able to meet the one hour mean time between assist requirement.

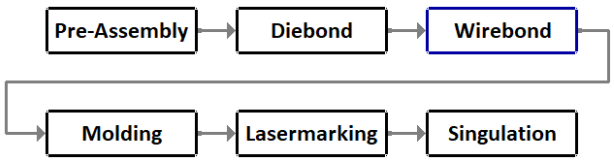

Fig. 3. Assembly process flow

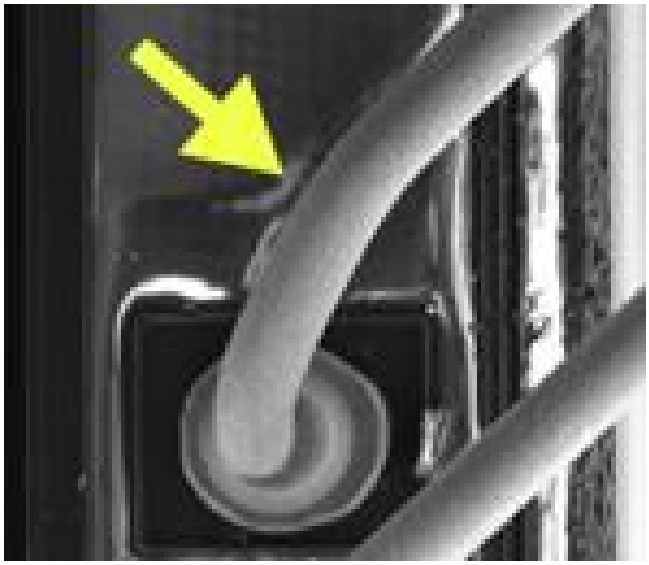

Fig. 4. Actual J-wire loop implementation

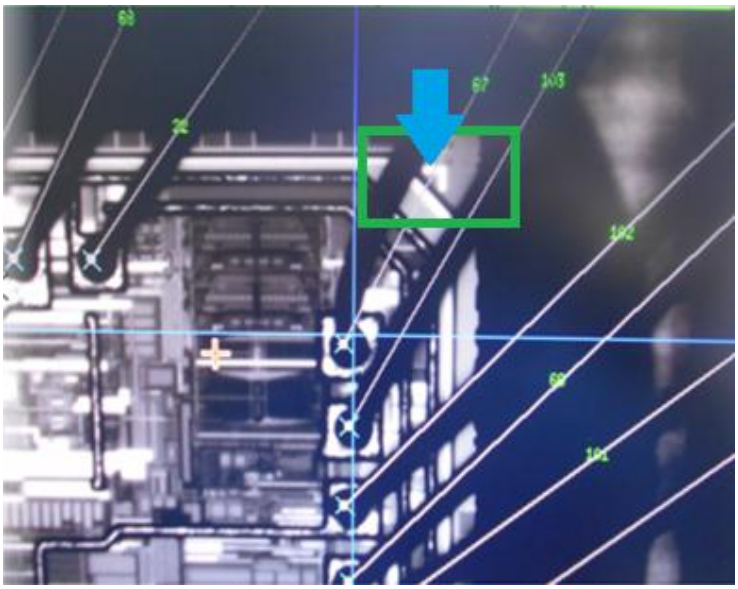

Fig. 5. Adjusted wirebond parameter to J-wire loop, resulting in visible L-fiducial

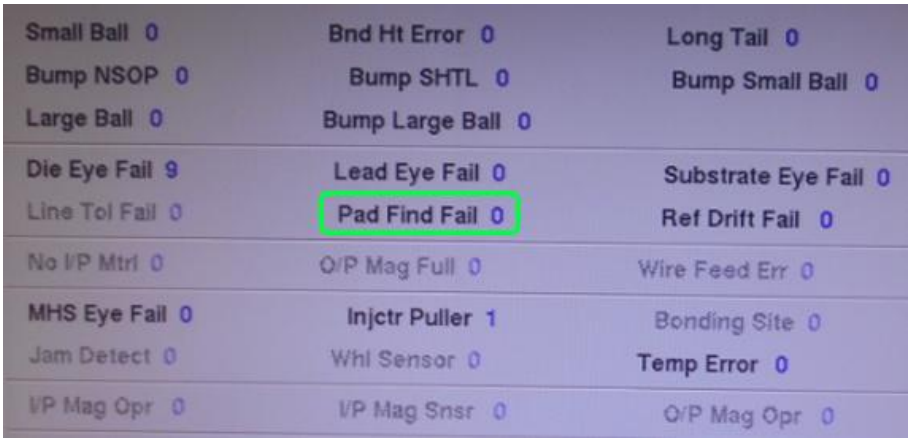

Fig. 6. Machine output showing no error on pattern recognition alignment

3. CONCLUSION

With the wirebond process optimization through the adjustment in the looping parameter, the wirebonding reference, which is the silicon die's L-fiducial, was ensured to be visible and not obstructed during the process. With this, a flawless wirebonding operation with two programs for the QFN-mr device was realized, with no pattern recognition alignment error and misplaced ball issues.

4. RECOMMENDATION

For future works, the enhanced wirebonding technique could be applied on other semiconductor devices with similar challenging configuration. Also, works and learnings discussed in [10-12] are helpful to further improve the wirebonding process.

DISCLAIMER

The products used for this research are commonly and predominantly used products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

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