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Hermetic chip-scale packaging using Au:Sn eutectic bonding for implantable devices

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Abstract

Advancements in miniaturisation and new capabilities of implantable devices impose a need for the development of compact, hermetic, and CMOS-compatible micro packaging methods. Gold-tin-based eutectic bonding presents the potential for achieving low-footprint seals with low permeability to moisture at process temperatures below 350 °C. This work describes a method for the deposition of Au:Sn eutectic alloy frames by sequential electroplating from commercially available solutions. Frames were bonded on the chip-level in the process of eutectic bonding. Bond quality was characterised through shear force measurements, scanning electron microscopy, visual inspection, and immersion tests. Characterisation of seals geometry, solder thickness, and bonding process parameters was evaluated, along with toxicity assessment of bonding layers to the human fibroblast cells. With a successful bond yield of over 70% and no cytotoxic effect, Au:Sn eutectic bonding appears as a suitable method for the protection of integrated circuitry in implantable applications.

Keywords: Au:Sn, eutectic, bonding, hermeticity, micropackaging, reliability, implant

(Some figures may appear in colour only in the online journal)

1. Introduction

One of the most critical design challenges in the growing sector of miniaturised, smart implantable devices is providing reliable packaging of small footprint and good hermeticity [1, 2]. Novel implantable devices ever-expanding capabilities more often include fully wireless communication and on-node data processing, thus imposing more rigourous requirements for device packaging [3]. Nowadays implant packages aside from ensuring small size, reliability, and biocompatibility, may additionally require complementary metal-oxide-semiconductor (CMOS) compatibility and transparency to the communication signals [4–6]. Until now, the majority of implants were packaged by encasing entire systems in metal or glass cases or by using thick outer coatings, mainly made of medical-grade silicones [2, 6, 7]. Typically, these solutions either do not provide an appropriate level of hermeticity or are too large and not fit for wireless systems with integrated electronics. At the same time, it is not certain whether standard IC insulation layers alone are sufficient

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in providing enough protection against the inherently wet and often corrosive character of the tissue environment over long time [8–10]. Recently, approaches of using thin, atomic layer deposition (ALD)-deposited high-K ceramic materials such as Hafnium Dioxide and multilayers of Silicon Dioxide with Hafnium Dioxide as a protective coating on neural implants have emerged [11, 12]. They hold the promise of thin, stable coatings; however, they would not solve the issue of mechanical stability of chips stressed by the tissue nor integration difficulty of more advanced microelectrode designs. For that reason, the prospect of hermetically enclosing implant electronics at a wafer- or chip-scale by using narrow seal rings with the addition of in-silicon feedthroughs is highly desirable [13].

From a myriad of bonding techniques available in electronics and micro-electromechanical systems (MEMS) packaging, only a few do not require high-temperature processing nor contain toxic materials while providing good seal hermeticity, thus making them applicable for implantable devices containing embedded ICs [14, 15]. To list a few, anodic bonding methods require non-CMOS-compatible high electrostatic fields, thermocompression, and glass frit bonding use very high temperatures, while the majority of solders contain copper and silver proven to be cytotoxic elements. Amongst all packaging methods, eutectic bonding is well-established and can be performed using relatively relaxed environmental parameters while the availability of several different eutectic compositions enables the choice of the one that would suit the application needs the best. In particular, solder sealing techniques achieve amongst the best hermeticity, as compared to anodic, direct and glass fusion bonding [16]. A clear advantage of metal-based sealing is the tolerance to substrate unevenness and very low permeability to moisture, superior to even those of silicon or glass [17].

While primarily used for die attach and flip-chip bonding in semiconductor and optoelectronics packaging, eutectic bonding can be also used for hermetic sealing [19, 20]. The concept relies on using a single solder frame at the interface of two substrates protecting circuitry and devices enclosed within. Since the joint's thickness and width are in the range of tens of microns or less, considerable design freedom and reduction in the package size can be achieved. Out of a number of eutectic compositions existing, the one particularly interesting for the application in implantable technologies is gold-tin metallurgy [21, 22]. This is thanks to Au:Sn favourable characteristics of high joint strength, fluxless processing, reliability, and moderate liquidus temperature of 278 °C. Alternatively, Au:Si has been proposed as an eutectic alloy employed in the packaging of implantable applications [19]. This is thanks to the biocompatibility of alloy's components and a relatively low eutectic temperature of 363 °C. However, gold-silicon alloy presents itself with challenges with right under layer metallisation choice and significant thermal stresses. As compared to gold-silicon, gold-tin eutectic is achieved with a much lower thermal load, whereas slight difference between thermal expansion coefficients of Si and AuSn makes it suitable for high-temperature devices.

Table 1. Selected applications of Au:Sn solder rings for hermetic sealing.

Application	Details	Year
Smart inertial MEMS sensor systems	- Chip-to-wafer integration - Au:Sn frame: 18 μm height, electroplated - Bonding: 300 °C, 6 kN force	2008 [32]
RF MEMS switch	- Wafer-level integration - Au:Sn frame: 5 μm height, electroplated - Bonding: 310 °C	2010 [33]
Piezoelectric silicon resonators	- Wafer- and array-level integration - Au:Sn frame: 4 μm height, electroplated	2011 [24]
MEMS microresonators and microbolometers	- Chip-level integration - Au:Sn frame: 20 μm, electroplated - Bonding: 340 °C	2013 [25]
MEMS timing devices	- Wafer-level integration - Au:Sn frame: 19 μm, electroplated - Bonding: 300 °C	2013 [23]

Au:Sn bonding has been already demonstrated for the packaging of MEMS devices, particularly for radio frequency (RF) and inertial applications (table 1) [23–25]. Gold-tin eutectic joining has been particularly popular and established in hermetic sealing of ceramic-metal packages that can house variety of MEMS sensors, also adapted for military use [16, 26–28]. Although, in order to utilise this method more widely and effectively, more studies on bond characteristics and reliability are needed, especially for implantable applications. To deliver a good quality seal, it is of much importance to control the deposition of eutectic composition correctly, as at exactly 80:20 Au:Sn ratio by weight (see figure 1) low eutectic temperature of the alloy is paired with desirable properties of Au_5Sn intermetallic phase [29, 30]. There are several possible methods for depositing gold-tin alloy (see figure 1), whereas the most popular and cost-effective approach is electrochemical deposition. This is typically achieved by means of alloy plating which suffers problems of short service life and solution stability [31]. To overcome that issue, composition plating can be executed by sequential electroplating, which involves using different chemical solutions to deposit each component of the eutectic alloy [30].

In this paper, we explore the effectiveness of tin-rich sequentially deposited Au–Sn alloy eutectic bonding for achieving high-quality, hermetic seals for chip-scale implantable devices. We investigate key parameters such as the influence of bond geometry, solder thickness and reflow parameters on bond mechanical properties and hermeticity. To establish a preliminary validation of biocompatibility critical for any implantable applications, the cytotoxicity of plating chemistry, as well as the alloy itself, were assessed by culturing human fibroblast cells on reflown samples.

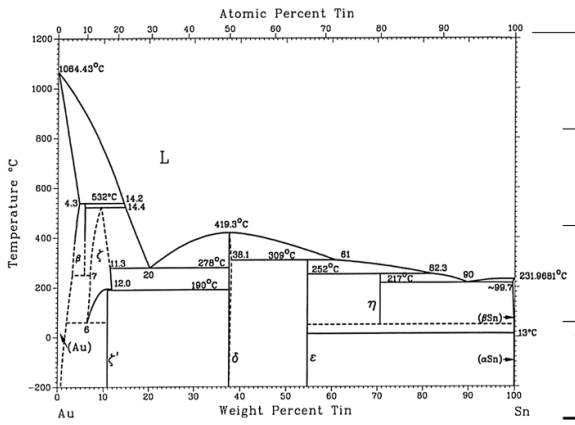

Figure 1. Left: Au:Sn binary phase diagram [18]. Right: most common Au:Sn solder deposition methods and their characteristics.

2. Materials and methods

All experiments were carried out in an academic cleanroom laboratory setting (Centre for Bio-Inspired Technology Cleanroom, Imperial College London and London Centre for Nanotechnology Cleanroom, Univeristy College London) using 4-inch, double side polished, 525 μm thick (100) silicon wafers of total thickness variation lesser than 2.3 μm. Substrates were processed in two batches, separately for lid and base die samples. All mask layers were custom designed so that cap wafers sealing rings match with those on the base wafers. Overall, two sample sizes (4 mm^2, 9 mm^2), with four widths (30 μm, 60 μm, 90 μm, 150 μm) and three different shapes (circular, rectangular, and chamfered) of seal rings have been tested. Eutectic stacks heights were electroplated to the heights of either 10 μm or 15 μm, which corresponds to Au(6 μm)–Sn(4 μm) and Au(9 μm)–Sn(6 μm) tin-rich compositions, respectively. The range of tested parameters was based on the previous literature (table 1) of the subject and project's constraints regarding the package size, which was to be kept smaller than 4 $\times$ 4 mm^2. Additionally, some of the geometries contained gold-only rectangular standoffs, placed either inside or outside of the seal rings (figure 2).

2.1. Fabrication of base and lid wafers

A simplified fabrication process flow is depicted in figure 3. Processing commenced with full RCA clean, after which lid wafers were oxidised with approximately 320 nm dry thermal silicon oxide and base wafers were coated with approximately 960 nm PECVD-deposited oxide (Mesc Multiplex 13 241 system, STS, UK). The difference in oxide thickness was chosen so that base wafers oxide layer thickness corresponds better to those on the BEOL layers used in CMOS chips. Next, adhesion layers of either Cr or Ti were sputtered (PVD75, K.Lesker, USA) to the thickness of 20 nm and directly followed by sputter deposition of 100 nm layer of Au, which would work as a seed layer for later electrodeposition steps. Subsequently, selected substrates were photolithographically patterned with 5 μm AZ 15nXT (115 CPS) photoresist to form an array of square-shaped openings which were then electroplated with gold to the height of 5 μm using parameters described in the later steps. This is to create gold standoffs near the solder lines which would work as possible spillage stoppers preventing full solder collapse during bonding. Then, the photoresist was stripped in heated MICROPOSIT Remover 1165, and substrates were cleaned in Acetone and Isopropanol baths followed by DI water rinse and nitrogen dry.

Until this point substrates intended for both base and lid of the package were processed the same. In the next step, lid wafers were photolithographically patterned with the shapes of seal rings in AZ1518 HS photoresist followed by differential etching away of previously sputtered Ti/Au layers and removal of photoresist in acetone. In the next step, lid wafers were again patterned with the use of SPR-220 photoresist to form central square openings used for the formation of central cavities. These cavities are to provide space for the placement of cut copper film pieces (in the future to be replaced by humidity sensors) used to evaluate bond hermeticity. After the removal of silicon dioxide in buffered hydrofluoric acid, cavities were etched down in the Bosch process to the depth of 200 (Multiplex Pro DRIE, SPTS, UK). Then, lid wafers were stripped of photoresist, solvent- cleaned, and diced into 4 and 9 mm^2 dies (DAD3230 dicing saw, DISCO Corporation, Japan).

After electroplating of spillage-stoppers, base wafers were sectioned into four pieces to separate wafer areas containing designs of different sizes. This was to avoid electroplating with starkly different local current densities across the wafer and thus allowing for better control of the deposition process. Then, base wafer sections underwent another photolithography to pattern outlines of seal rings. For that, a thicker version of the previously used photoresist AZ 15nXT (450 CPS) of the thickness of 120% of desired plated deposit thickness was used. Thereafter, substrates were sequentially electroplated with gold and tin layers. Once that was achieved, the photoresist was stripped, and wafers solvent cleaned. Next, samples underwent selective etching of thin films of adhesion and seed layers in gold, chromium, and titanium etchants (KI, $HClO_4$:$(NH_4)_2[Ce(NO_3)_6]$, HF; respectively) thus leaving only layers of deposited solder on the silicon dioxide base. Finally, base wafer sections were diced to singulate dies of

a)

Process parameter:	Solder Ring Width [µm]	Solder Ring Height [µm]	Solder Ring Geometry	Bonding Force [N]	Process Temperature Treatment Profile
Values Evaluated:	30 60 90 150	10 15 20 30	• Circle • Square • Chamfered Square	0 10 20 30 40	• (FR) Fast direct ramp-up, long hold time • (PFR)Fast direct ramp-up and long hold time on pre-reflown samples • (SR) Ramp-up with intermediate pre-reflow step at 200 °C, short hold time

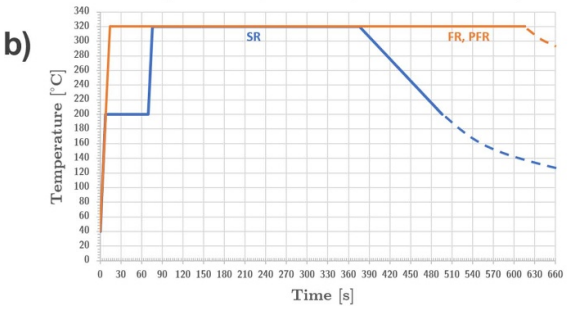

Figure 2. (a) An overview of process parameters tested in the study. (b) Reflow temperature profiles evaluated. (c) Evaluated seal geometries of the square, chamfered square, and round frames.

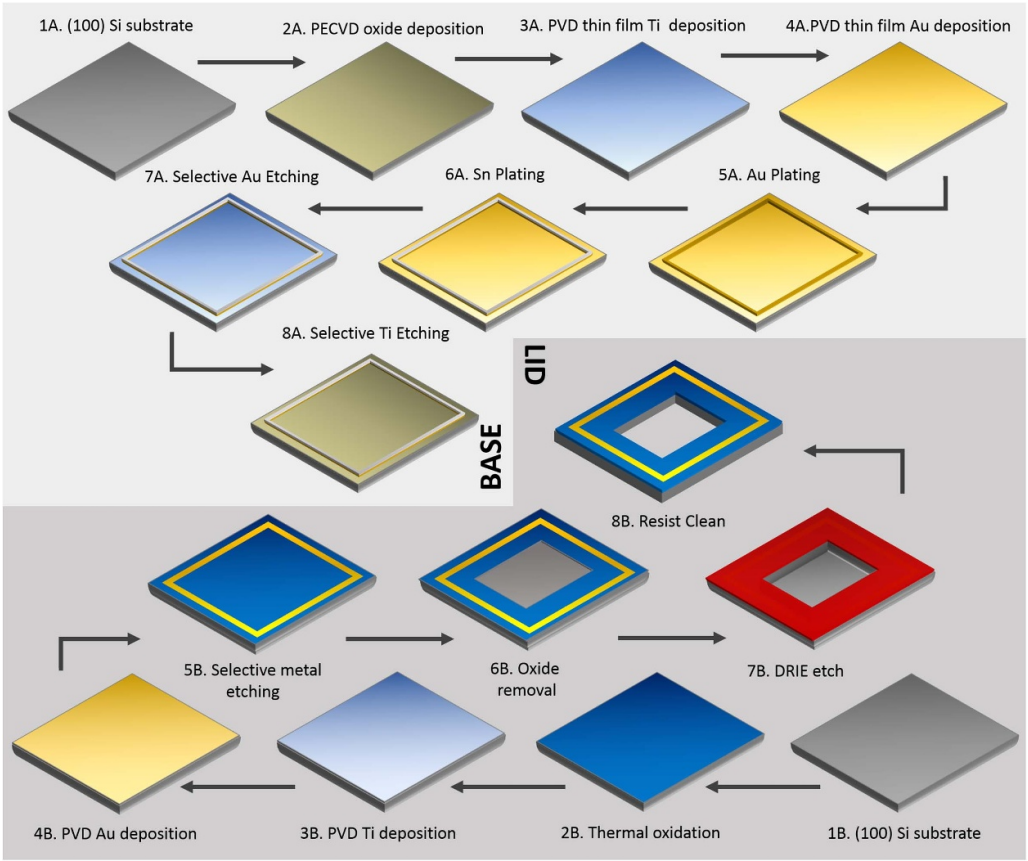

Figure 3. An overview of base (above) and lid (below) wafers fabrication process flow.

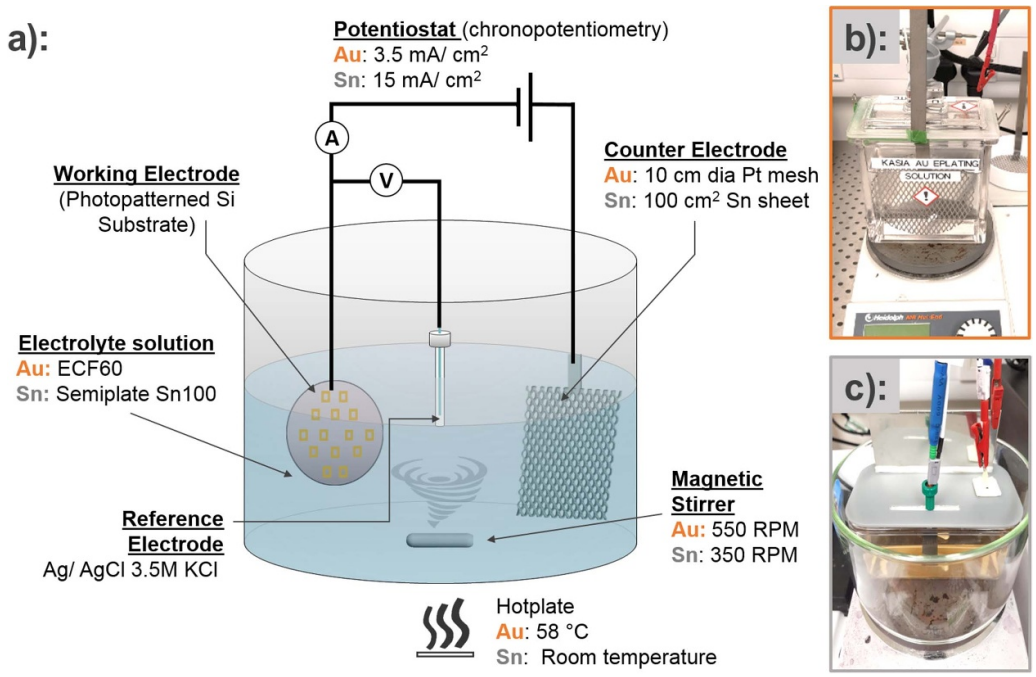

Figure 4. (a) Sketch of setup used for electrochemical deposition of Au and Sn layers. (b) Picture of Au-electroplating setup realisation. (c) Picture of Sn-electroplating setup realisation.

sizes corresponding to those diced from lid wafers, and exact solder heights were measured by contact profilometry. One set of samples was then annealed in vacuum oven at 200 °C for 4 h.

2.2. Au:Sn alloy sequential electrochemical deposition

For all described electroplating experiments, custom electrochemical deposition setup was assembled, which is depicted in figure 4. Electrochemical workstation in a chronopotentiometry mode (Versastat-3-400, Princeton Applied Research, USA) was employed as a power source. To ensure better control over plating current, depositions were conducted in a three-electrode system, using double junction 3.5 KCl-filled silver/silver chloride (Ag/AgCl) electrode as a reference. Electrical between working electrode terminal and samples was realised via custom made spring-loaded contacts. The thickness of grown deposits was regularly monitored by measuring grown layer ex-situ using stylus profilometer(Dektak X, Veeco, USA).

For gold electrochemical deposition, proprietary sulphite based ECF60 (Metalor, UK) gold bath, without additives or grain refiners, was used. This chemistry was chosen because sulphite-based Au-plating solutions are known to produce layers of ductile, soft pure gold with good throwing power and are safer to use than cyanide-based chemistry. Electroplating was carried out against a 10 cm diameter platinised titanium mesh counter electrode at an operating temperature of 58 °C. The exact plating current density value was chosen based on the manufacturer's recommendations and previous literature on the subject at 3.5 mA cm^{-2} where built-in stress of deposited gold layer is the lowest. To limit the formation of an ion-depleted solution layer in the cathode vicinity over time, the solution was continuously stirred by immersed magnetic pellet with a spin speed of 550 rpm s^{-1}. Throughout the gold electroplating process, the counter electrode and samples were kept 5 cm apart, the distance defined by the geometry of the plating vessel.

Electroplating of tin was performed using proprietary methanesulphonic acid-based NB Semiplate Sn100 solution (Microchemicals GmbH, Germany) producing matte tin layers of high purity and low internal stresses. The deposition was performed using 100 cm^2 99.9% tin sheet counter electrode, at room temperature. The plating solution was constantly stirred with 350 rpm min^{-1} speed using a magnetic pellet to disperse hydrogen gas bubbles forming during deposition and to aid the flow of fresh solution to the sample's surface. Counter and working electrodes were kept at a constant distance of 3.5 cm from each other, a gap defined by the geometry of the plating vessel.

2.3. Bonding process

To test the effectiveness of sequential electrodeposition to form eutectic composition, as well as to evaluate bond characteristics, corresponding lid and base dies were bonded together using die bonder (Lambda Fineplacer, Finetech, Germany). In total, 110 sample pairs were processed. All samples were bonded at least three weeks after the last electroplating step. Shortly before bonding, sample pairs were briefly cleaned in acetone and isopropanol and carefully dried with a nitrogen gun to remove any possible dicing-induced contamination. Several samples were additionally equipped with small cut out of copper film placed inside lid's cavity to monitor hermeticity of formed seal. Lid and base dies were aligned at full separation using bonders's optical system, brought

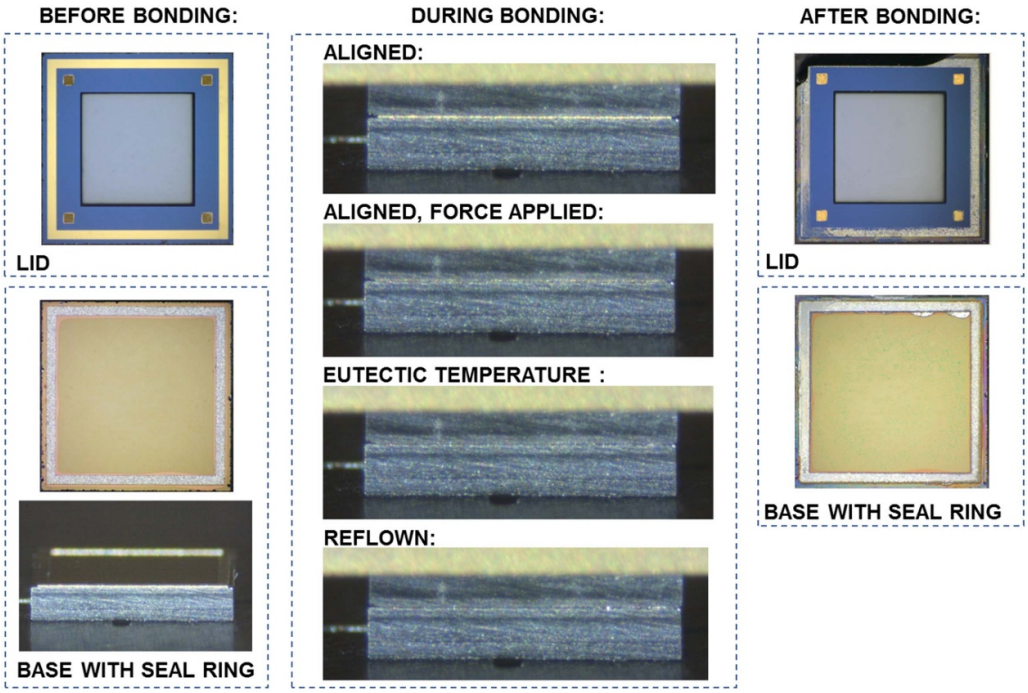

Figure 5. Microscope photographs of lid and base chips' surface as seen before bonding (left) and after reflow and following shear tests (right). The side profile of the chip stack as seen during the bonding procedure (centre). Solder collapse and change in colour appearance of solder are observed.

together to direct contact and subjected to the force of value ranging from 0 to 40 N per solder ring. The bonding was done by applying two different temperature profiles, depending on the tested batch (orange and blue lines on temperature profile in figure 2(b). Batch PFR containing samples prereflown in the vacuum oven and batch FR were bonded by applying 320 °C on the sides of both base and lid dies, with the ramp rate of 20 K s^{-1} and held at the maximum temperature for 10 min, after which heating was turned off and the sample was allowed to return to room temperature without any external cooling. Samples from batch SR were reflown by applying 200 °C to both base and lid dies, with the ramp rate of 20 K s^{-1} for 60 s followed by a further ramp-up to 320 °C bonding temperature where they were held for 5 min. After that samples were first actively cooled to 200 °C and then allowed to further cool down without any external aids. Once the bonded pairs achieved room temperature, the force was removed, and samples were removed from the bonder for characterisation. Throughout the entire bonding process, samples were observed for the eutectic temperature, premature melting, spillages, and bond collapse via the side camera (figure 5).

2.4. Post-bonding characterisation

The objectives for an implantable device package are the protection of the device against an external, humid environment of living and constantly mobile environment over a long time. Thus, the effectiveness of the bonding approach was characterised with a focus on shear strength, hermeticity, cell response to sealing material, and the overall yield of the bonding process. Hermeticity was qualitatively evaluated by the evaluation of the change in surface oxidation of copper films as exposed to a wet environment in immersion tests. Of several leak detection methods available to use as a measure of hermeticity, the copper test was chosen, because of its straightforwardness and accessibility at the time of experiment. Gold-standard methods, such as the helium leak test, typically do not offer sufficient resolution for the device's submillimetre cavity size without system adaptations such as pirani gauge or absolute sensor's offset voltage [16, 27, 34]. In the future, integration of on-chip humidity sensor would provide more quantitative measure of hermeticity [35, 36]. Directly after bonding, two sample sets containing enclosed copper film pieces were placed in the deionised water for 12 weeks at room temperature, and in phosphate buffered saline for seven weeks at 55 °C along with the exposed copper control samples. The liquid was changed weekly. Then, samples were debonded and enclosed copper pieces evaluated for the change in appearance. The colour change of the copper film could indicate the progress of oxidation caused by moisture ingress to the inside of a bonded sample.

Strength of single seal frames was measured by mean of shear tests. The tests were carried out using force gauge (FH500, Sauter, Germany) fitted with custom 3D printed holders to which the backside surface of measured samples was carefully fixed using fast-setting adhesive (see figure 6). Adhesive layer was thin enough to prevent it from bleeding into the interface between lid and base dies. The load was applied with the approximate rate of 0.02 mm s^{-1} until samples debonded at the interface and the maximum measured force was registered. The shear strength was then calculated by

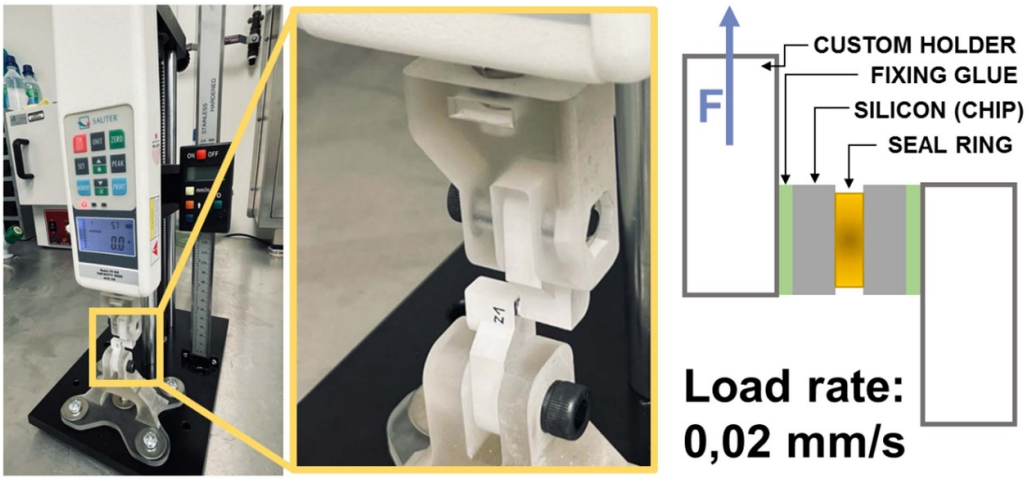

Figure 6. Shear test setup.

dividing the recorded force by the total bonded area. Samples were subsequently inspected with optical microscope and scanning electron microscope to examine for the extent of possible spillages as well as to evaluate the fracture mechanism of broken bonds.

2.5. Cell viability assessment

Selected nine reflown and debonded samples were used as substrates for the human fibroblast cell viability and cytotoxic assessment. Samples used were sectioned off wafers before dicing therefore they were of larger size, each containing several seal rings. This was to evaluate the cytotoxic response of human fibroblast cell line to the Au:Sn solder in eutectic composition as deposited using sequential electroplating from sulphite and methanesulfonic acid-based gold and tin plating solution chemistries. Biocompatibility was assessed via analysis of cell morphology as inspected by scanning electron microscopy. Initially, samples were sterilised by exposing to UV light for 20 min followed by washing with PBS three times before adding to cell culture medium. Next, cultured human fibroblast cells were employed in cell experiments to ascertain the cytotoxicity and cellular response to the fabricated layers. The cell line used in this experiment-fibroblast cell BJ (ATCC® CRL-2522™), was purchased from ATCC and cultured in Dulbecco's modified Eagle's medium containing 10% heat-activated fetal bovine serum with 1% penicillin-streptomycin antibiotics (Pen-strep). Subsequently, the cells were seeded and cultured on reflown Au:Sn substrates and placed in Petri dishes with a seeding density of 750 000 cells cm^{-2}. The cells were incubated in the medium for 24, 48, and 72 h at 37 °C, and 5% CO_2 while they were examined every 12 h.

3. Results

The majority of samples tested exhibited very good mechanical characteristics of produced joints. Across various geometries and parameters examined, the overall yield of the bonding process was 73%. Out of the total of 110 sample pairs processed, 24% have produced seals with mechanical characteristics too weak to allow to conduct shear strength measurement and debonded upon normal handling. Within the well-bonded group, 12% of samples exhibited shear strength values below the minimum as described by MIL-STD-883G military standard for die-attach calculated per total bond area [37], thus reducing the total yield of bonding process across the range of parameters tested to approximately 64%.

No correlation was observed between the shape of the seal lines and the resulting measured bond strength. For the frames of the same width, all shapes (circle, square, chamfered square) exhibited similar ranges of measured shear strength values. Thus, when mechanical properties are of the main importance, the shape of solder rings are not relevant parameter. Variations in seal behaviour were observed for bond frames of different widths, as 150 μm lines exhibited lower shear strength values as compared to thinner 90 and 60 μm wide lines of the same height. This could be explained by wider frames having larger Au:Sn interface surface area, thus more availability for premature gold diffusion and the formation of high-temperature intermetallic compounds. On the other hand, wider frame widths were found more robust in maintaining the hermeticity of packages. In immersion tests, all 150 μm and the majority (80%) of 90 μm-wide frames kept enclosed copper pieces intact after 12 weeks in water. Leakages were observed commonly for thinner frames as a result of a higher probability of misalignment between lid and base dies. In thinner frames, the appearance of voids has more of a detrimental impact because of the smaller volume of the solder available for package protection. All copper pieces enclosed by 30 μm wide Au:Sn seal frames showed signs of exposure to water as observed by the copper colour changes (figure 7). Such occurrence was not observed in all 30 μm wide PBS-immersed samples, where the third of thinnest frames provided the barrier against moisture ingress. From mechanical stability as well as hermeticity perspective, optimum seal geometries found out to work the best for

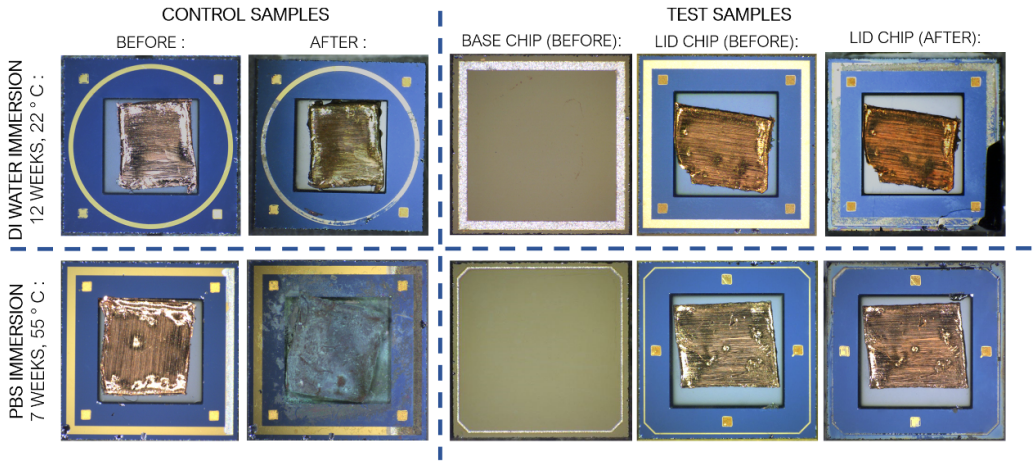

Figure 7. Comparison of an oxidation level of copper film immersed for 12 weeks in deionised water at room temperature (upper row) and immersed for seven weeks in phosphate buffered saline solution at 55 °C (lower row). Left side of the figure represents view of control samples(exposed to moisture) and right side samples sealed by Au:Sn frame.

the die sizes examined were those of middle range of widths (60 and 90 μm).

A structural parameter that exhibited more influence on the shear strength values was stack height. Deposited layers were higher than 10 μm to ensure the proper ratio of gold to tin is maintained. When sequentially electroplating gold and tin from two separate solutions, two distinct metallic layers of different grain sizes were achieved. Whereas gold's layers are deposited to form smooth layers of small grains and compact microstructure, deposition of tin from methane sulfonic acid produced films of comparably more developed morphology. Micro roughness of tin, resulting from its grain size, leads to difficulties in accurate measurement of the deposited layer, thus controlling the right eutectic ratio, especially for thin solder layers. When chosen eutectic height is tall enough, the grain size measurement error becomes insignificant thus allowing for successful Au:Sn proportion deposition. Any premature Au:Sn intermixing and resultant consumption of metals in favour of the formation of intermetallic compounds different to Au_2Sn is minimised with thicker layers deposited. All samples of as-deposited Au:Sn heights of 10 and 15 μm achieved eutectic composition, as observed by the presence of a single uniform metal phase in post-reflow SEM images and in-situ observed reflow temperature.

Four different eutectic height groups were evaluated: SL with 10 μm of as-plated eutectic height on the base die; SH with 15 μm of as-plated eutectic height on the base die; DL with 10 μm of as-plated eutectic height on both base and lid dies (total 20 μm) and DL with 15 μm of as-plated eutectic height on both base and lip dies (total of 30 μm). Additionally, the SL2 group consisting of dies with 7 μm-high Au:Sn eutectic on the base die with Cr adhesion layer was tested (figure 8). The latter group yielded the lowest shear strength values as the chromium layer was proven insufficient to provide an adequate level of adhesion for grown eutectic. What is more, selective etching of chromium thin film from die surface during the last step of processing led to the premature rapid oxidation of the electroplated tin surface, thus further

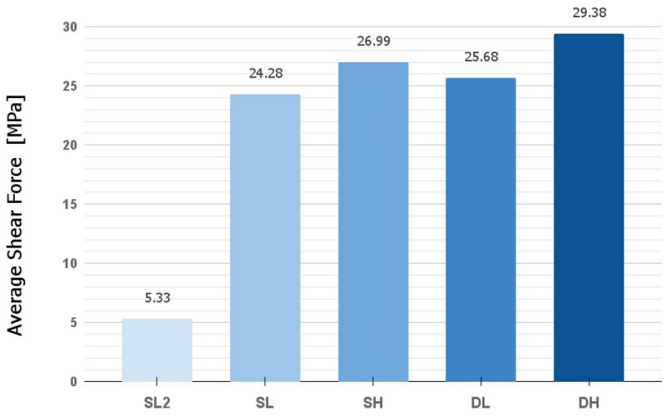

Figure 8. Average shear force for samples of different as-plated solder heights. SL-10 μm total solder on-base die only; SH-15 μm total solder on-base die only; DL-20 μm total solder on base and lid dies; DL- μm total solder on base and lid dies.

hindering subsequent bonding steps. For that reason, results from group SL2 are not included in the overall statistics of the experiment. For the remaining samples with Titanium deposited as an adhesion layer, the average shear force measured was larger for higher thicknesses of the deposited solder. For the groups of dies with solder stack present only on one die, the variation in average shear strength between solder heights of 10 and 15 μm was only 2.71 MPa . Doubling the amount of solder by depositing eutectic stack on both base and lid wafers led to an average shear strength increase of 1.4 MPa for samples with double-10 μm stacks, and 2.39 MPa for samples with double-15 μm stacks. It must be noted that when double solder height is considered, a considerably larger extent of excess solder spill-out was observed for samples of all geometries. Furthermore, all double-height-bonded samples exhibited different shear fracture modes, mainly breaking at the bond interface. Considering the increased cost and complexity of double-stacked samples against an only minor increase in shear strength, it was concluded stacks deposited

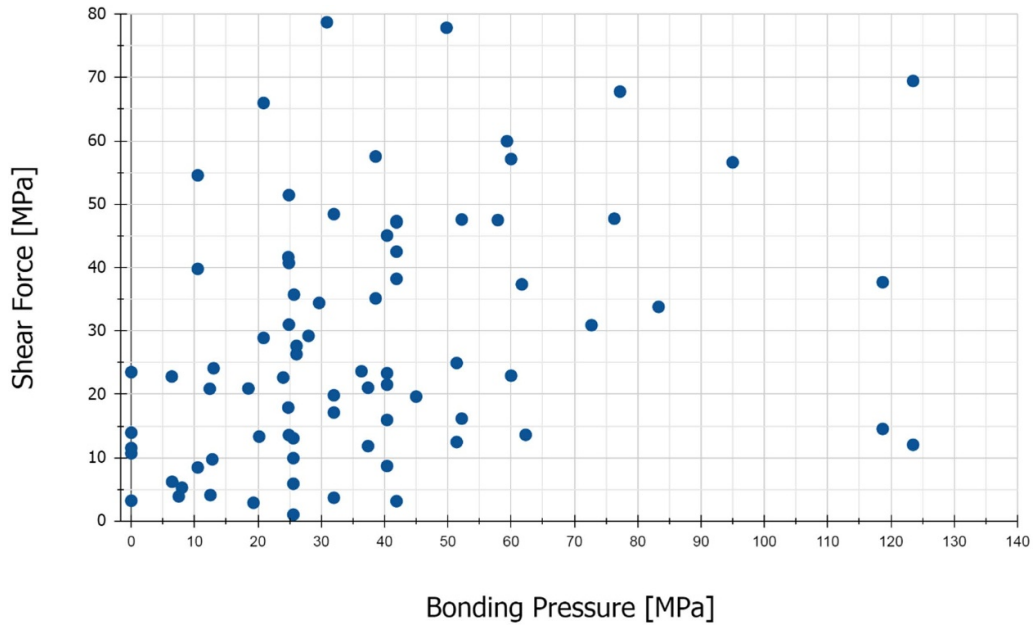

Figure 9. Measured shear force in relation to pressure applied to the sample during the bonding procedure.

on only one of the package dies were sufficient in providing a reliable seal.

Analysis of measured shear force against pressure applied onto the seal frames during the bonding process has shown that with an increase of bonding pressure, achievable shear strength is on average higher (figure 9). This is in part caused by improved mixing of solder phases during reflow under pressure. Applying pressure aids in the removal of voids as well as in the improvement of wetting of solder to the substrate, however, it causes bond line widening and increases the possibility of solder squeeze out and spillages. Very high bonding pressures were also found to cause minor shifts in dies alignment when the surface of the bonder was not perfectly levelled. On the other hand, minimal or no bonding pressure was found to be a parameter used in 40% of all samples from the group of the weakest bonds that failed upon regular handling. Nonetheless, applying low to moderate pressures along with the right adjustments of other bond parameters, such as eutectic height, makes it feasible to attain shear strengths in the range above 20 MPa, which are applicable for intended implantable purposes.

Clear differentiation between the total yield of well-bonded samples can be observed for dies reflown with different temperature profiles (figure 10). Samples that were heat-treated in a vacuum oven before final reflow successfully bonded only in 36% cases, while using the same temperature profile on samples without any prior annealing led to an increase in yield to 78% of well-sealed samples. Typically, pre-reflow annealing is employed to increase the bondability of as-deposited layers over time by minimising the rate of diffusion of Au into Sn and the formation of unwanted intermetallics [38]. However, in our case annealing negatively impacted bonding process yield likely as a result of increased Ti adhesion layer consumption. Application of intermediate annealing step at 200 °C directly before reflow above eutectic temperature also had a negative impact on process yield. Thus preferably from the process yield perspective, reflow at a temperature above eutectic should occur as soon as possible, with as fast as possible ramp up any without any prolonged exposure to temperatures above melting temperature of Sn.

Figure 11 represents SEM pictures of various fracture modes identified after shear testing. For a large number of samples analysed, the transfer of Ti:Au thin film bi-layer from the surface of the silicon onto the bond frame was observed. This indicates the failure occurring at the interface of solidified solder and adhesion layer, pointing out the good mechanical stability and quality of the bond. The exact location for that type of failure could occur both at the interface between Au:Sn and Ti, as well as Ti and SiO_2. The high occurrence rate of this fracture mode may indicate the need for improvements of the adhesion layer to limit the dissolution of Ti into the solder. Another type of fracture identified is the one within the solid Si itself, represented as fragmentary remains of the corresponding sample from the pair attached to the solder frame. This fracture type was the second most observed and shows the bond strength surpassing fracture strengths of silicon/silicon oxide die. The least observed fracture mode was the one occurring within the bulk of the bond frame bulk itself, usually caused by either the solder imperfections such as voids or by the wrong composition of the solder and therefore phases non-uniformity.

Cell adhesion and morphology were observed by SEM on the surface of reflown Au:Sn eutectic after culturing for 1, 2, and 3 days. Representative surfaces after incubation in the cell culture medium are shown in (figure 12). No cytotoxicity effect on fibroblasts structure could be observed between

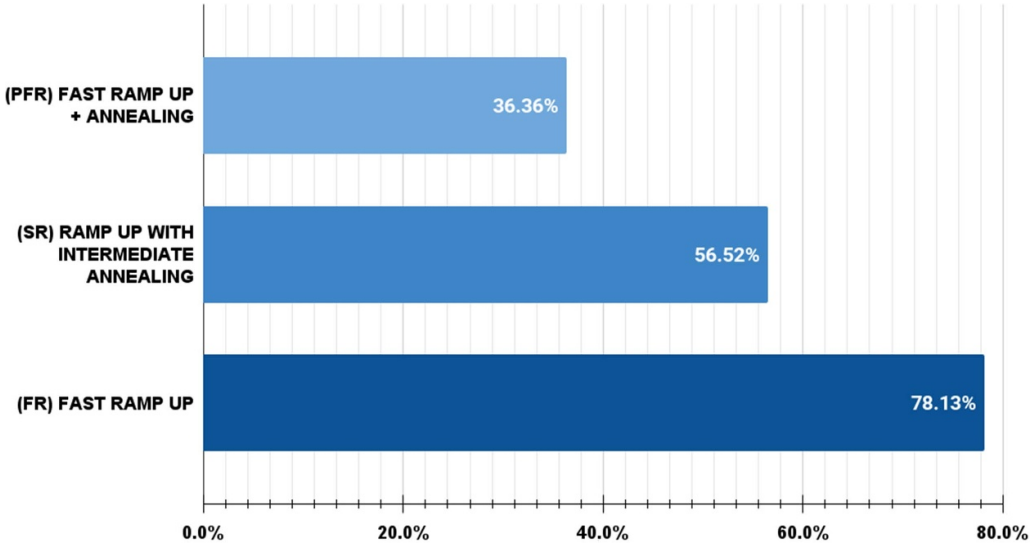

Figure 10. The average shear force between samples reflown with different temperature profiles, with or without pre-bonding annealing step.

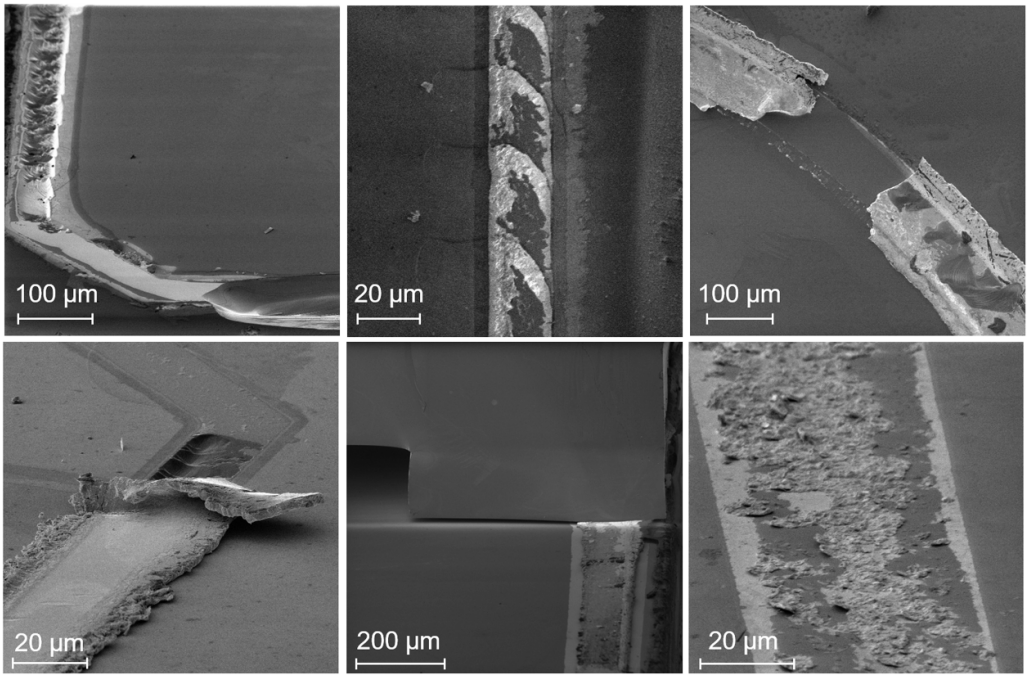

Figure 11. SEM pictures of fracture modes observed at the debonded interface of samples following shear testing.

time points of 1, 2 and 3 days, with cells consistently exhibiting normal, spindle-like morphology. Cell density exponentially increased over the course of incubation time. Continued proliferation of the fibroblast after 3 days has created a tissue-like structure on the surface of samples which suggest the biocompatibility and non-cytotoxicity of the substrates [39, 40]. An untreated area of the samples were considered as control. Increasing numbers of fibroblasts attached to the surface and in the contact with each other were observed. The clear preference of cellular attachment on the silicon oxide as compared to the reflown Au:Sn was noted, with a sparser cellular layer covering solder lines. Nonetheless, fibroblasts present on the solder frames remained of healthy morphology, with only a few individual cells exhibiting round shape. The density of fibroblasts coverage after culturing for more than 3 days was high enough to cover the majority of sample surfaces, proving no cytotoxic effect of sequentially electroplated Au:Sn solder.

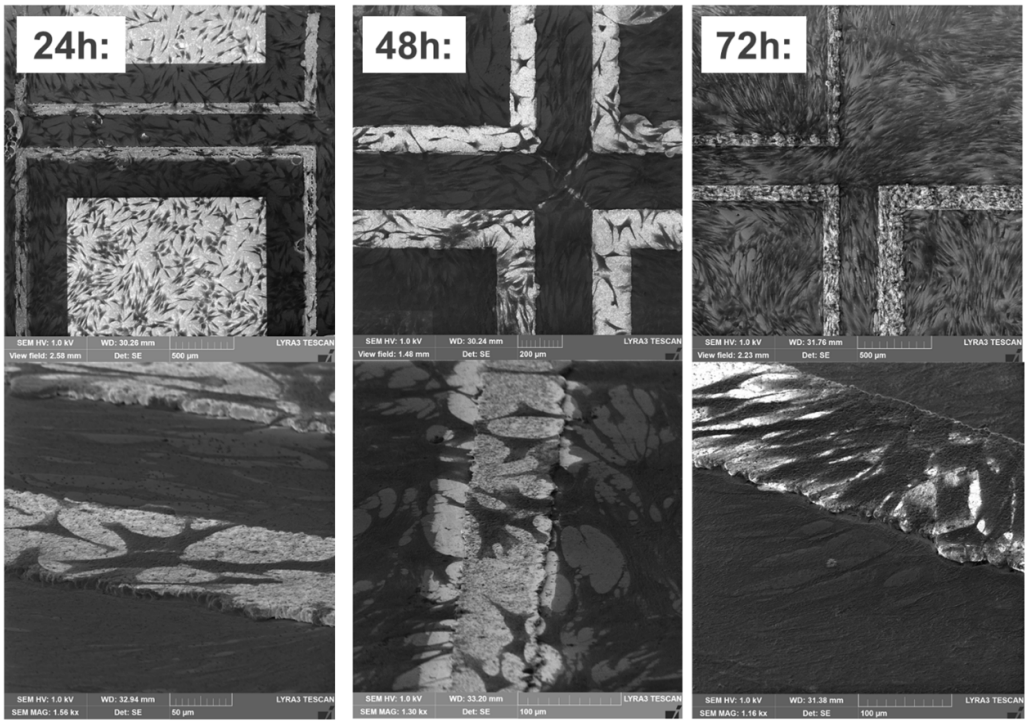

Figure 12. SEM pictures of reflown chip surface with Au:Sn solder lines used for fibroblast cell culturing after 24, 28, and 72 h of cell culture.

4. Conclusions

A method for creating strong, hermetic seals using Au:Sn alloy sequentially electroplated from commercially available solutions is presented. Fabrication of eutectic frames is performed using standard microfabrication methods and thanks to the maximum process temperature of 320 °C can be applied to temperature-sensitive devices, such as CMOS microelectronics dies. The use of electroplating over other methods of alloy deposition allows for a parallel formation of multiple solder frames with great geometry control while the choice of plating sequentially significantly reduces problems of plating solution stability and shelf life. The wide availability of considerably low toxicity gold and tin electroplating chemistry makes the process both cost and time effective. However, because of different Au and Sn layer morphology, it can be applied only where a thicker solder layer can be tolerated. Bonding tests with varying parameters of applied temperature, reflow profile, and frame geometry along with immersion tests have shown the possibility of this method to create an enclosed, mechanically robust hermetic environment. Across all geometries and process parameters tested, the average measured bonding strength was over 28 MPa with a bonding success yield of 73%. The dominant shear fracture observed was at the interface of the adhesion layer, pointing to the need for improvement under solder metallisation. Nonetheless, even with only Ti/Au stack underneath, samples have exhibited excellent mechanical properties. Analysis of average bond shear force between samples having either single- or double-sided solder rings has shown no need for solder presence on both base and lid dies. This means that for applications where CMOS dies are to be used as a base there would be no need for on-chip electroplating, as solder frames on separately processed lid chips would be sufficient in providing a high-quality seal. Immersion tests conducted for the duration of three months have shown no signs of moisture penetration in samples sealed with frames of 90 and 150 μm width, whereas the majority of thinner 30 μm-wide frames have exhibited leakage. As a result of cell culture experiments, Au:Sn reflown layers have not shown signs of high toxicity to the biological environment. It would be of future interest to investigate different under-layer metallisation to further improve the mechanical stability of seals.

Unquestionably one of the most significant trends for the future of implantable devices is miniaturisation. The designs of novel implantables are characterised by complicated architectures and expectations of possibility of high yield manufacturing. Therefore, the device's design for manufacturability, including packaging methodology, ought to be considered from the very beginning. Presented Au:Sn-based eutectic sealing can be applied to a variety of substrate materials and used on a larger scale, also at wafer-level, thus significantly improving the process throughput. In the future, it is envisaged to expand the abovementioned work to full wafer-scale experiments. The influence on the bonding process of substrate non-homogeneities and dicing-induced stresses could then be estimated.

The presented method appears suitable packaging approach for the protection of integrated circuitry in implantable applications or any other application where a device must be protected from an external operating environment. The possibility to hermetically seal IC-electronics within an implant, in a simple and robust way, as with using Au:Sn eutectic, can pave the

way to expand the horizon of implantable devices into the new areas. Such narrow, hermetic seals do not require any specialised microfabrication approaches, are not toxic, and provide long-term robustness.

Once combined with the right approach to the challenges of power and data transmission out of implants [13], correct packaging methodology could enable future devices to be potentially safer, less invasive, and easier to implant [41, 42].

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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