Journal of Engineering Research and Reports

20(3): 32-36, 2021; Article no.JERR.65046
ISSN: 2582-2926

Die Crack Resolution through Pick-up Process Optimization for BGA Package

R. Rodriguez[1], E. Graycochea Jr.[1*], F. R. Gomez[1] and E. Manalo[1]

[1]New Product Development & Introduction, STMicroelectronics, Inc., Calamba City, Laguna 4027, Philippines.

Authors' contributions

This work was carried out in collaboration among the authors. All authors read, reviewed, and approved the final manuscript.

Article Information

DOI: 10.9734/JERR/2021/v20i317277
Editor(s):
(1) Dr. David Armando Contreras-Solorio, Autonomous University of Zacatecas, Mexico.
Reviewers:
(1) Jamal M. Rzaij, University of Anbar, Iraq.
(2) Emilio Jiménez Macías, University of La Rioja, Spain.
Complete Peer review History: http://www.sdiarticle4.com/review-history/65046

Original Research Article

Received 30 November 2020
Accepted 01 February 2021
Published 25 February 2021

ABSTRACT

With the new devices and new technologies in the semiconductor industry are getting more challenging to process because issues are unavoidable especially on thin dies. The paper is focused on the improvement done on a ball grid array (BGA) substrate package assembly to address the quantity of rejection of die crack during die picking at the die attach process station. High pick force and high needle top height found out during the pick-up process is the main root cause of die crack. Parameter optimization particularly for die picking with the combination of pick force and needle top height parameter was done to eliminate this type of issue after the die attaches process. With the die attach process improvement, a reduction of 100 percent of die crack occurrence was successfully achieved. For future works, the improvement and learnings could be used for devices with similar constraints.

Keywords: BGA; die crack; pick force; pick-up process; silicon die.

1. INTRODUCTION

To keep up with the fast-changing technology and development in the semiconductor industry, one should be flexible and resourceful in adapting to change in order to have a very good impression from the eventual customer. This is one of the biggest challenges for any

**Corresponding author: Email: edwin.graycocheajr@st.com;*

semiconductor company to maintain its competitive market position and value. Contrariwise, failure to provide customer expectations will result in possible business failure.

BGA packaging technology is continuously developed and improved to deliver high quality and robust products for various applications. A common direction of semiconductor manufacturing companies is to increase the production yields and maintain high quality products while minimizing wastage and assembly rejections. With the new and continuous technology trends and breakthroughs, challenges in assembly manufacturing are unavoidable [1-4]. Die attach process is responsible for picking silicon die on a wafer tape to a substrate or carrier. This paper presents a solution and improvement done to process this type of assembly manufacturing reject which is a silicon die crack by optimizing the pick parameter of pick force and needle top height. Pick force is the amount of additional pressure applied during picking the silicon die with the help of vacuum to picked while needle top height is a parameter wherein the needle push upward or eject the silicon die. Fig. 1 shows the actual unit of die crack.

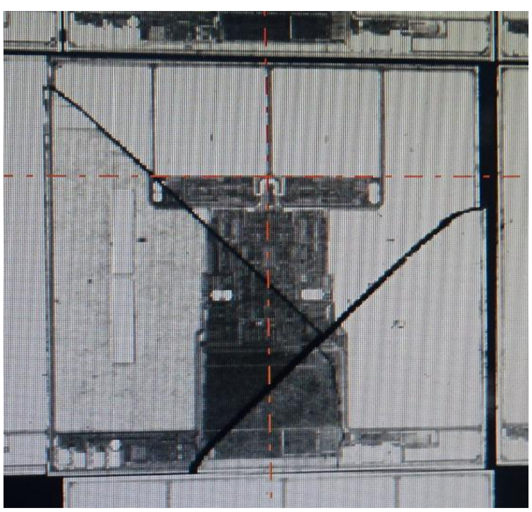


Fig. 1. Actual reject manifestation of die crack

2. METHODS AND RESULTS

A typical assembly process flow for the BGA package device in focus, starting with the pre-assembly to singulation process is shown in Fig. 2. Highlighted is the process where the issue was encountered. Important to note that assembly process flow varies with the die technology and package design requirements [5-8].

Die crack was the top major assembly reject in the die attach process for the device in focus, and this was seen during the lot processing on the development stage of the device. One of the challenges is to process this type of technology with a thin die thickness of 70 microns (μm). This die crack reject is caused by a high needle top height and high pick force during the die picking process. Fig. 3 illustrates the pick-up process.

The process starts with picking the semiconductor die from a wafer silicon tape. The most common method used in die bonding: first, is when the ejector needle pushes up the target semiconductor die from the wafer silicon tape; then is picked by a rubber tip or pick-up tool as shown in Fig. 3. With this picking process, Fig. 4A shows the die crack pick process while Fig. 4B is the actual die crack during picking the silicon die. High pick force and needle top height found out that this parameter fully induced on the defect manifestation of die crack.

An improved and enhanced process solution in die attach process is widely done with the combination of pick force and needle top height parameter optimization. The needle used is usually a plastic type and this was normally used in all semiconductor industries. With the combination of pick force and needle top height parameter optimization, no die crack occurrence is seen after implementing the improvement in the die attach process. Table 1 shares the evaluation on pick force and needle top height. The result of the needle top height parameter from 0.4mm to 0.7mm has evidence of die crack while 0.2mm to 0.3mm is the best parameter to use without die crack and the die is properly picked and placed on the lead frame or substrate carrier. The result of pick force parameter from 1.1N (newton) to 2N has an evidence of die crack while 0.5N to 1N is the best parameter to used without die crack.

The optimized parameter would eventually have a good reliability test and a good die shear strength. With this optimized pick for and needle top height would properly place on the lead frame or substrate carrier without die crack occurrence. Die crack occurrence was succesfully eliminated as shown in Fig. 5. Note that actual parts per million (PPM) level are intentionally not shown due to confidentiality.

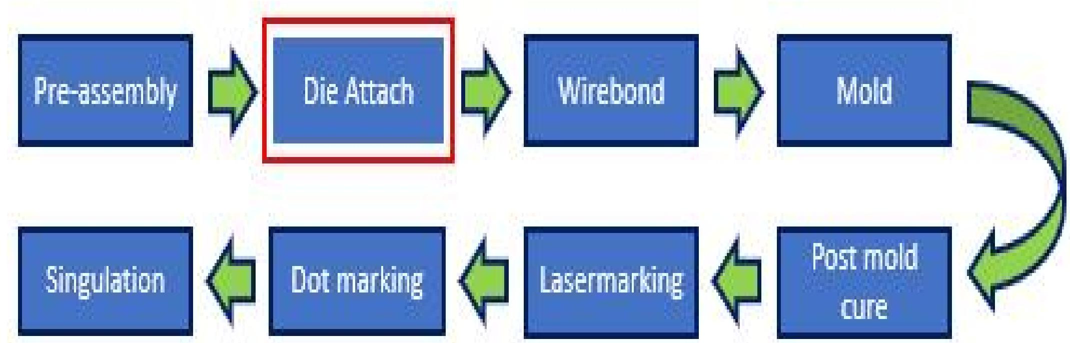


Fig. 2. Device process flow

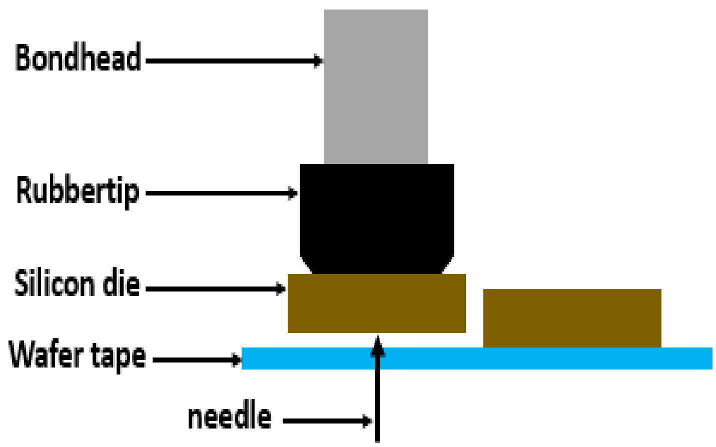


Fig. 3. Pick-up process representation

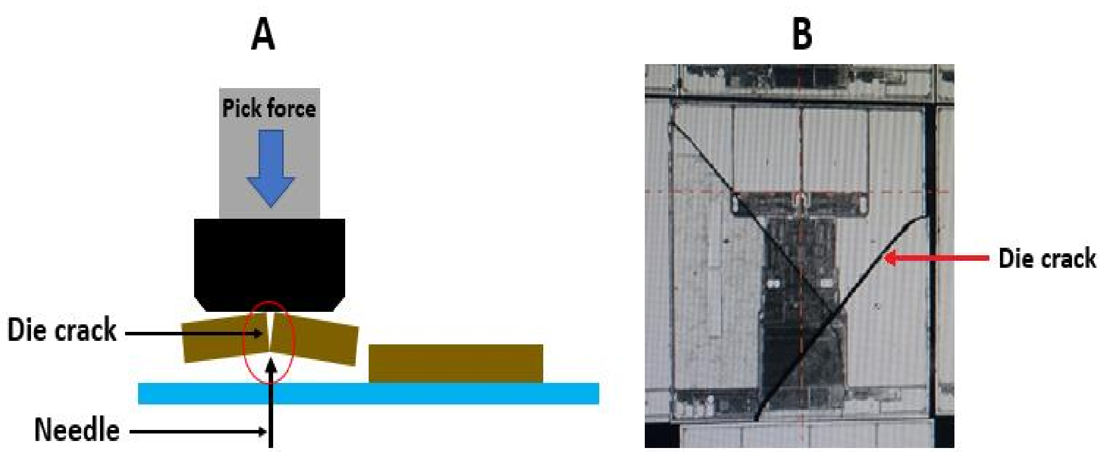
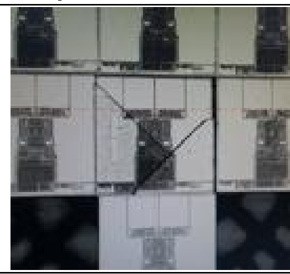
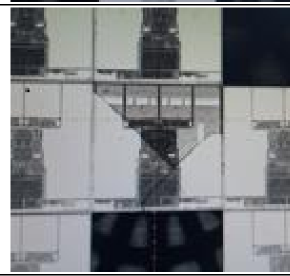
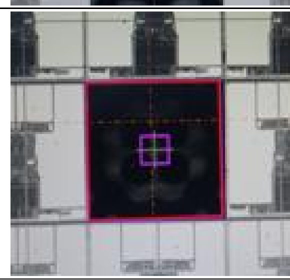


Fig. 4. A) Die crack pick-up process; B) Actual die crack during picking of silicon die

Table 1. Evaluation table of pick force and needle top height

Parameter	Response	Remarks
Needle top height: 0.6mm – 0.7mm Pick force: 1.6N – 2N		Observed die crack
Needle top height: 0.4mm – 0.5mm Pick force: 1.1N – 1.5N		Observed die crack
Needle top height: 0.2mm – 0.3mm Pick force: 0.5N – 1N		No die crack

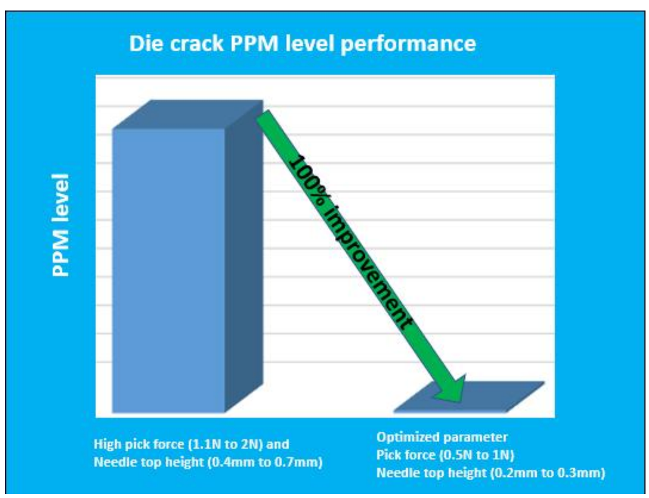


Fig. 5. Improvement in the die crack reduction performance

3. CONCLUSION AND RECOMMENDATIONS

Die crack mitigation was successfully realized through the comprehensive die attach process characterization and optimization for BGA device. Parameter optimization on pick-up process with the combination of pick force and needle top height parameter were employed, resulting to 100 percent improvement on die crack occurrence reduction. The pick parameter optimization in this study could be used for future works on other BGA products with similar configurations. Comparison of existing works and other studies should also be included for added analysis, as well as the mechanical tests of the prepared samples. Worth noting is that continuous process improvement is important to sustain the high-quality performance of semiconductor products and their assembly manufacturing. Studies and learnings shared in [9-12] would help reinforce the robustness and optimization of assembly processes particularly at die attach process.

DISCLAIMER

The products used for this research are commonly and predominantly used products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

ACKNOWLEDGEMENT

The authors would like to thank the Management Team and the New Product Development & Introduction (NPD-I) colleagues for the great support.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Liu Y et al. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference, Singapore; 2008.
2. Saha S. Emerging business trends in the semiconductor industry. Proceedings of PICMET '13: Technology Management in the IT-Driven Services (PICMET). USA. 2013;2744-2748.
3. Hwang J. Solder paste in electronics packaging: technology and applications in surface mount, hybrid circuits, and components assembly. Ven Nostrand Reinhold, New York, USA; 1989.
4. Yeap LL. Meeting the assembly challenges in new semiconductor packaging trend. 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT). Malaysia. 2010;1-5.
5. Coombs C, Holden H. Printed circuits handbook. 7th ed., McGraw-Hill Education, USA; 2016.
6. Harper C. Electronic packaging and interconnection handbook. 4th ed. McGraw-Hill Education, USA; 2004.
7. Nenni D, McLellan P. Fabless: the transformation of the semiconductor industry. CreateSpace Independent Publishing Platform, USA; 2014.
8. May GS, Spanos CJ. Fundamentals of semiconductor manufacturing and process control. 1st ed., Wiley-IEEE Press, USA; 2006.
9. Kahler J et al. Pick-and-place silver sintering die attach of small-area chips. IEEE Transactions on Components, Packaging and Manufacturing Technology. 2012;2(2).
10. Rodriguez R, Gomez FR. Rubber-tip design improvement for die crack elimination at diebond process. Journal of Engineering Research and Reports. 2020;12(2):1-5.
11. Xian TS, Nanthakumar P. Dicing die attach challenges at multi die stack packages. 35th IEEE/CPMT International Electronics Manufacturing Technology Conference (IEMT). Malaysia. 2012;1-5.
12. Abdullah S et al. Dicing die attach film for 3D stacked die qfn package. 32nd IEEE/CPMT International Electronic Manufacturing Technology Symposium. USA. 2007;73-75.

Peer-review history:
The peer review history for this paper can be accessed here:
http://www.sdiarticle4.com/review-history/65046